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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,889	09/04/2003	Makoto Yoshida	501.37959CC2	4939

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/653,889	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 17, lines 17-18, the phrase "a bit line formed on said first opening which **is formed on said element isolation region**" is not described in the specification and shown in the figure.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phase "a bit line formed on said first opening which is formed on said second insulating film" renders the claim indefinite. It is not clear which element is formed on the second insulating film –a bit line or the first opening--.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 11-18, insofar clear, are rejected under 35 U.S.C. 102(e) as being anticipated by Kasai et al. [U.S. Patent 6,448,597] previously applied.

With respect to claim 11, Kasai et al. (figs. 14A-14F, cols. 5-9) discloses a semiconductor integrated circuit device, comprising:

a semiconductor substrate (12) with an active region defined by an element isolation region (13), word lines (14) extending in a first direction over said active region such that gate electrodes (34) of metal insulator semiconductor field effect transistors (MISFETS) are electrically coupled to said word lines (14), semiconductor regions formed in said active region extending in a second direction perpendicular to the first direction such that said semiconductor regions (36) serve as a source region or a drain region of each MISFET;

a first insulating film (71A) and second insulating film (54) covering said active region, said word lines (14) and said semiconductor regions (36);

a first opening (79) formed in said first insulating film (71A) such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region (13) (fig. 14B);

a second opening formed in said second insulating film (54) under said first opening (79) such that a diameter of said second opening in the first direction is less than that of said first opening and such that said second opening reaches said semiconductor regions (fig. 14B);

a conductive material (74) buried in said first opening (79) and in said second opening; and

a bit line (38) formed on said first opening (79) such that said bit line is electrically coupled to said conductive material (34) and extends to cross said word lines (see fig. 8).

With respect to claim 12, Kasai et al. further discloses:

a capacitor element (52) formed over said first insulating film (71A);

a third opening (79) formed in said first insulating film (71A) and said second insulating film (54) to reach other semiconductor region (36); and

a conductive material (74) buried in said third opening (79),

wherein said capacitor element (52)is electrically coupled to the other semiconductor region (36) through said conductive material (74) buried in said third opening (79) (see fig. 14F and col. 8, lines 64-67).

With respect to claim 13, Kasai et al. discloses that a memory cell of a dynamic random access memory is comprised of said MISFET (14) and said capacitor element (52) (see the Abstract).

With respect to claim 14, Kasai et al. (figs. 14A-14F, cols. 5-9] discloses a semiconductor integrated circuit device, comprising:

a semiconductor substrate (12) with an active region defined by an element isolation region (13), word lines (14) extending in a first direction over said active region extending in a second direction perpendicular to the first direction such that gate electrodes (34) of metal insulator semiconductor field effect transistors (MISFETS) are electrically coupled to said word lines (14), semiconductor regions formed in said active region such that said semiconductor regions (36) serve as a source region or a drain region of each MISFET;

a first insulating film (71A) and second insulating film (54) covering said active region, said word lines (14) and said semiconductor regions (36) (fig. 14B);

a first opening (79) formed in said first insulating film (71A) such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region (13);

a second opening formed in said second insulating film under said first opening (79) such that a diameter of said second opening in said first direction is less than that of said first opening (79), and such that said second opening reaches said semiconductor regions (fig. 14B);

a third opening (79) formed in said first insulating film (71A) and second insulating film (54) to reach other semiconductor region (36);

a conductive material (74) buried in said first opening, said second opening, and said third opening; and

a bit line (38) formed on said first opening (79) such that said bit line is electrically coupled to said conductive material (34) and extends to cross said word lines (see fig. 8).

With respect to claim 15, Kasai et al. further discloses:

a capacitor element (52) formed over said first insulating film (71A),

wherein said capacitor element (52)is electrically coupled to the other semiconductor region (36) through said conductive material (74) buried in said third opening (79) (see fig. 14F and col. 8, lines 64-67).

With respect to claim 16, Kasai et al. discloses that a memory cell of a dynamic random access memory is comprised of said MISFET (14) and said capacitor element (52) (see the Abstract).

With respect to claim 17, Kasai et al. (figs. 14A-14F, cols. 5-9) discloses a semiconductor integrated circuit device, comprising:

a semiconductor substrate (12) with an active region defined by an element isolation region (13), word lines (14) extending in a first direction over said active region such that gate electrodes (34) of metal insulator semiconductor field effect transistors (MISFETS) are electrically coupled to said word lines (14), semiconductor regions formed in said active region extending in a second direction perpendicular to the first direction such that said semiconductor regions (36) serve as a source region or a drain region of each MISFET;

a first insulating film (71A) covering said active region, said word lines (14) and said semiconductor regions (36);

a first opening (79) formed in said first insulating film (71A) such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region (13) and such that said first opening (79) reaches said semiconductor regions (fig. 14B);

a conductive material (74) buried in said first opening (79); and

a bit line (38) formed on said first opening (79) such that said bit line is electrically coupled to said conductive material (34) and extends to cross said word lines (see fig. 8).

With respect to claim 18, Kasai et al. discloses that a memory cell of a dynamic random access memory is comprised of said MISFET (14) and said capacitor element (52) formed over said first insulating film (see the Abstract).

Response to Arguments

6. Applicant's arguments filed 11/30/2004 have been fully considered but they are not persuasive.

Applicant argues that Kasai does not disclose or suggest Applicants' claimed "first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region"; "second opening formed in said second insulating film under said first opening such that a diameter of said second opening in said first direction is less than that of said first opening, and such that said second opening reaches said semiconductor regions" and "bit line formed on said first opening which is formed on said second insulating film such that said bit line is electrically coupled to said conductive material and extends to cross said word lines".

Applicant's arguments are not persuasive because Kasai clearly discloses that a first opening (79) formed in said first insulating film (71A) such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region (13) (fig. 14B); a second opening formed in said second insulating film (54) under said first opening (79) such that a diameter of said second opening in the first direction is less than that of said first

opening and such that said second opening reaches said semiconductor regions (fig. 14B); and a bit line (38) formed on said first opening (79) which is formed on said second insulating film (54) such that said bit line is electrically coupled to said conductive material (34) and extends to cross said word lines (see fig. 8).

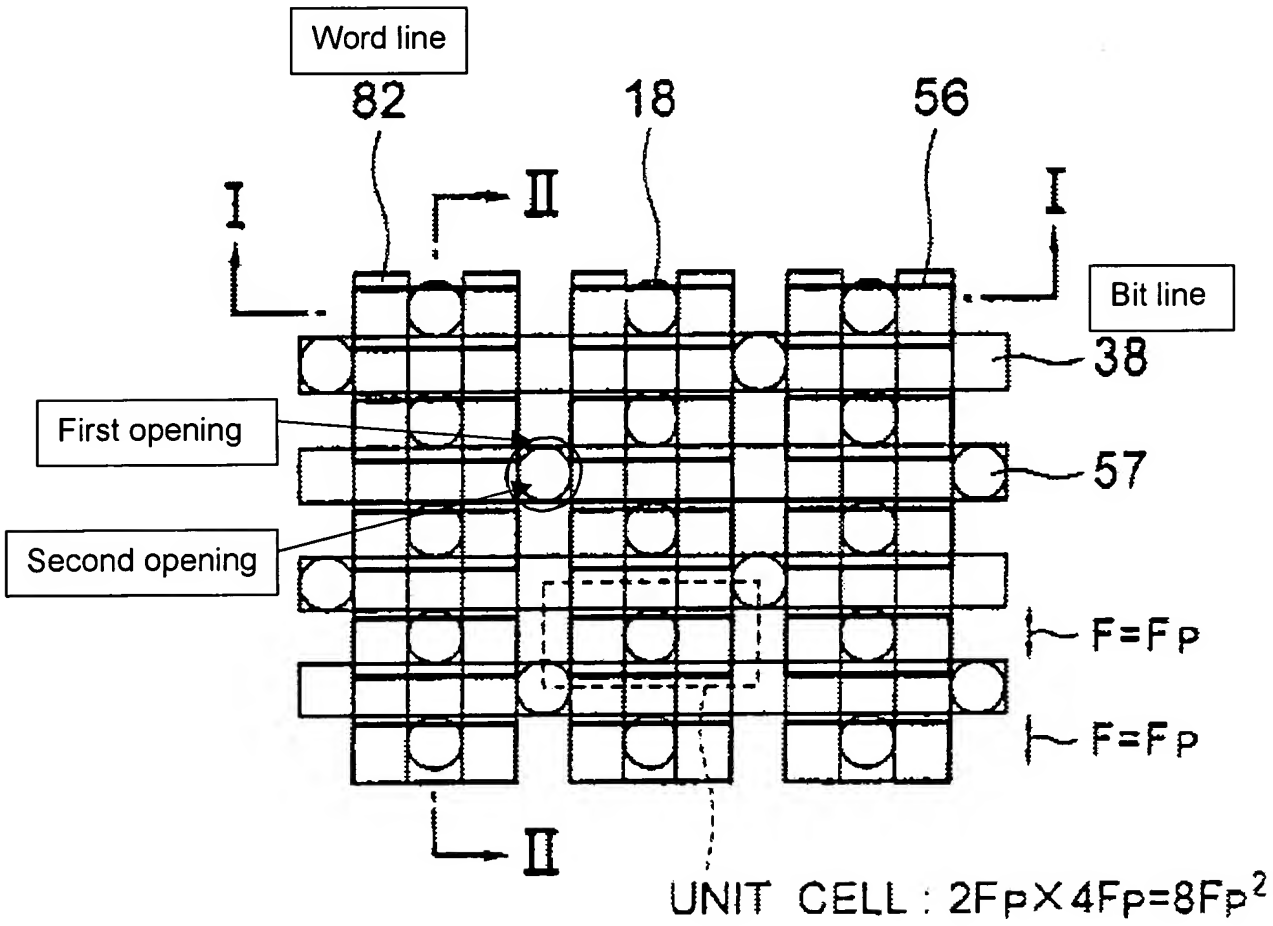
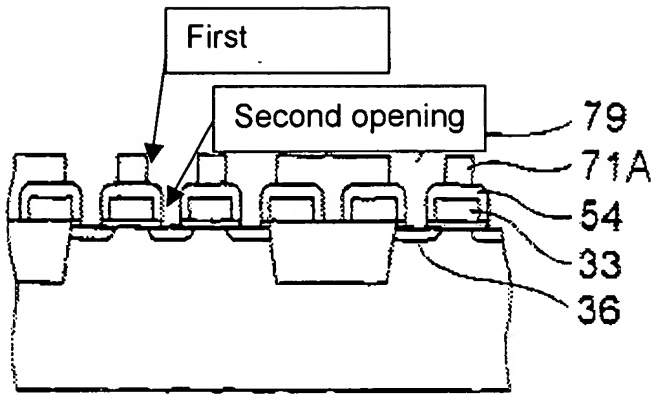


FIG. 8

FIG. 14B



Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER